The GSI Event Driven TDC ASIC GET4 V1.23

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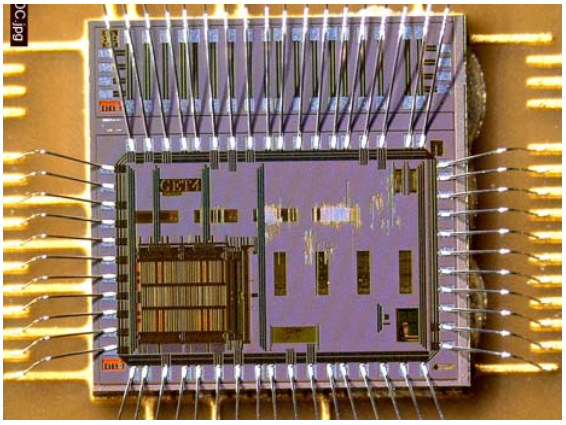

Figure 1: Die Picture of the GET4 ASIC.

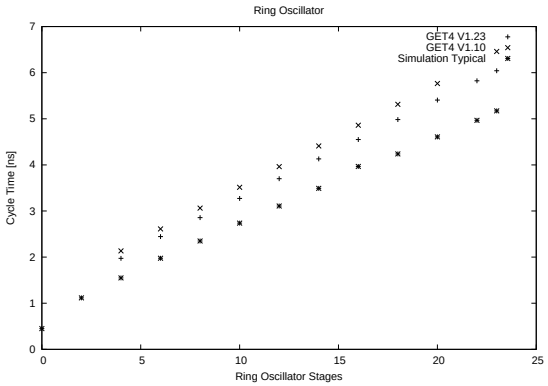

Figure 2: Measured and simulated cycle time of the internal ring oscillator.

Introduction

In the scientific report 2012[1] first results of the GET4 V1.10 ASIC the first fully equiped event driven TDC prototype taped out in 2012 (see figure 1) are reported. The excellent performance regarding timing precision was reported but also some minor bugs are mentioned.
To fix these bugs in 2013 a second iteration was taped out and tested. First results are presented in this report.

Logic Revision

Two faults of the read out logic have been found in GET4 V1.10[2]. A *sync*-flag in the epoch events was not set correctly and a setup and hold timing violation leads to data errors in the 24 bit read out mode with data rates below 160 MBit/s. To clear these faults the struture of the 24 bit serialiser was modified and the vhdl source code was corrected. Tests of GET4 V1.23 have shown that the *sync* flag now is set correctly and the 24 bit serialiser works correctly at all data rates.

Process Variations

The main problem of GET4 V1.10 was caused by process variation during the MPW run. The internal delays were significantly larger than in simulation and in previous ASICs. Figure 2 show the measurement results of a ring oscillator with configurable length which is integrated on the GET4 ASIC in comparison to simulation results in typical corner.

The measured cycle times of GET4 V1.10 as well as of GET4 V1.23 are significantly larger than the simulated times. The increment per stage of cycle times of V1.10 is about 6 % larger than that of V1.23. This unusual large delay of V1.10 caused several problems in getting the DLL into lock state as well as in data transfer from the TDC core to the read out logic. These problems are discussed in detail in [2]

To overcome the last mentioned problem a configurable delay element was integrated in the data transfer clock to adjust the clock phase for best fit with process speed. An increase of core voltage by 10 % as it was needed for operation of GET4 V1.10 is no longer required for GET4 V1.23.

Outlook

In the meantime also the TDC perfomance of GET4 V1.10 could be confirmed with GET4 V1.23. For detector tests with RPC timing detectors additional GET4 V1.23 ASICs will be bonded on PCBs to test the performance of the GET4 TDC in the 2014 GSI beam time as well as in long term cosmic tests.

References

[1] H. Flemming, H. Deppe, “The GSI Event driven TDC GET4 V1”, GSI Scientific Report 2012

[2] H. Flemming, “Results of GET4 Tests Known Bugs and Performance”, Talk given in the weekly CSEE meeting https://wiki.gsi.de/foswiki/pub/EE/EEMeetVortragArch/GET4V1.10Bugs.pdf

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